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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: P/647-141

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 10/009244

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/03230	19 May 2000	11 June 1999

TITLE OF INVENTION: SPEECH SWITCHING APPARATUS

APPLICANT(S) FOR DO/EO/US: Toshiyuki NOMURA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. [X] The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. [X] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [X] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [X] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [X] Other items or information:
    Print EFS Form
    Intl. Prelim. Exam. Report
    Cover sheet of published PCT Intl. appln.
    6 Drawing Sheets (Figs. 1-7)
    6 References

EXPRESS MAIL CERTIFICATE

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Dorothy Jenkins
Signature

December 6, 2001
Date of Signature

U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 10/009244	INTERNATIONAL APPLICATION NO. PCT/JP00/03230	ATTORNEY'S DOCKET NUMBER P/647-141

17. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):	CALCULATIONS	PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1,040.00		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO 890.00		
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International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) 710.00		
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CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	14 - 20 =	0	X $18.00	$	
Independent claims	4 - 3 =	1	x 84.00	$ 84.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ 280.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 974.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$	
SUBTOTAL =				$ 974.00	
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TOTAL NATIONAL FEE =				$ 974.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 1,014.00	
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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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Specification

Speech Switching Apparatus

Technical Field

The present invention relates to a speech encoding/decoding apparatus and, more particularly, to a speech switching apparatus for switching one of a plurality of speech signals.

Background Art

Conventionally, speech is transmitted on a transmission path on which the bit rate changes by using an encoding method of adjusting the quality of a reconstructed speech signal by adapting an encoding bit rate to the transmission path bit rate by increasing/decreasing the bandwidth of the speech signal in accordance with the transmission path bit rate. The present inventor has already proposed a speech encoding/decoding apparatus in Japanese Patent Laid-Open No. 9-202475, as a speech encoding apparatus for generating N + 1 signals by changing the sampling frequency of an input speech signal, in hierarchically encoding the speech signal, and simultaneously multiplexing N-level indexes representing linear predictive coefficients, pitches, multipath signals, and gains which are obtained by sequentially encoding the input speech signal and the signals obtained by changing the sampling frequency in increasing order of sampling

frequency, and a speech decoding apparatus for hierarchically changing the sampling frequency of a reconstructed signal in accordance with the bit rate at which decoding is performed. In this apparatus, a first CELP (Code Excited Linear Prediction) encoding circuit for receiving the signal obtained by down-sampling an input signal using a down-sampling circuit outputs an encoded output to a second CELP encoding circuit, the second CELP encoding circuit encodes the input signal on the basis of the encoded output from the first CELP encoding circuit, a multiplexer outputs the encoded outputs from the first and second CELP encoding circuits in the form of a bit stream, a demultiplexer outputs the encoded output obtained by the first CELP encoding circuit from the bit stream to a first CELP decoding circuit when a control signal has a low bit rate, and extracts part of the output obtained by the first CELP encoding circuit and the output obtained by the second CELP encoding circuit from the bit stream, when the control signal has a high bit rate, to output them to a second CELP decoding circuit so as to output them through a switching circuit.

On the decoding side, the bandwidth of a reconstructed speech signal, i.e., the sampling frequency of a decoded speech signal, changes in accordance with the bit rate at the time of reception. When a user is to hear a sampled speech signal, a

sampling frequency must be set for conversion processing from a digital signal to an analog signal. In this case, in order to switch and reconstruct speech signals having different sampling frequencies, sampling frequencies must be set/changed. During this sampling frequency setting/changing processing, interruptions tend to occur in reconstructed speech.

The operation of a conventional speech switching apparatus will be described with reference to Fig. 7. The speech switching apparatus receives two types of speech signals (first and second digital speech signals) sampled with two different sampling frequencies (e.g., 8 kHz and 16 kHz), together with a control signal, and switching and reconstructing the first and second speech signals in accordance with the control signal.

In this case, the control signal is a signal for giving an instruction to reconstruct a specific one of the two types of speech signals.

A switching circuit 103 receives first and second speech signals and control signal, and switches and outputs the two types of speech signals to a D/A conversion circuit 112 at the switching timing designated by the control signal.

The D/A conversion circuit 112 sets the sampling frequency of the speech signal designated by the control signal, converts the input digital signal into an analog signal, and outputs it.

In the above conventional speech switching apparatus, in switching and reconstructing speech signals having different sampling frequencies, the sampling frequency in the D/A conversion circuit must be set/changed. During the setting/changing processing, interruptions occur in the reconstructed speech.

The present invention has therefore been made in consideration of the above problems, and has as its object to provide a speech switching apparatus which can reduce strange sounds produced when a plurality of different speech signals are reconstructed/switched.

Disclosure of Invention

In order to achieve the above object, according to the present invention, there is provided a speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising at least one sampling frequency conversion circuit for converting a sampling frequency of at least one of the plurality of input signals, a delay adjustment circuit for adjusting a phase of the input signal of the plurality of input signals, whose sampling frequency is converted by the sampling frequency

conversion circuit and a phase of the remaining input signal, and outputting the signals, and a switching circuit for selecting one of a plurality of output signals from the delay adjustment circuit in accordance with the control signal.

In this case, the delay adjustment circuit may make an adjustment to match the phase of the signal whose sampling frequency is converted to the phase of the remaining input signal.

The switching circuit may switch outputs at a timing set in consideration of a delay time in the delay adjustment circuit with respect to a switching timing designated by the control signal.

According to the present invention, there is provided a speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising a plurality of sampling frequency conversion circuits for converting sampling frequencies of the plurality of input signals to a predetermined frequency, a delay adjustment circuit for adjusting phases between output signals from the plurality of sampling frequency conversion circuits and outputting the signals, and a

switching circuit for selecting one signal from a plurality of output signals from the delay adjustment circuit in accordance with the control signal.

In this case, the delay adjustment circuit may make an adjustment to match the phase of the signal whose sampling frequency is converted to the phase of the remaining input signal.

In addition, the switching circuit may switch outputs at a timing set in consideration of a delay time in the delay adjustment circuit with respect to a switching timing designated by the control signal.

According to the present invention, there is provided a speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising at least one sampling frequency conversion circuit for converting a sampling frequency of at least one of the plurality of input signals, a delay adjustment circuit for adjusting a phase of the input signal of the plurality of input signals, whose sampling frequency is converted by the sampling frequency conversion circuit and a phase of the remaining input signal, and outputting the signals, an addition circuit

for selecting and weighting two signals from a plurality of output signals from the delay adjustment circuit in accordance with the control signal, and a switching circuit for selecting one signal from a plurality of output signals from the delay adjustment circuit and an output signal from the addition circuit in accordance with the control signal.

In this case, the switching circuit may switch a signal before switching of output signals from the delay adjustment circuit to an output signal from the addition circuit at a timing set in consideration of a delay time in the delay adjustment circuit from a switching timing designated by the control signal, outputs the output signal from the addition circuit for a predetermined interval, and then output the signal after switching.

According to the present invention, there provided a speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising a plurality of sampling frequency conversion circuits for converting sampling frequencies of the plurality of input signals to a predetermined frequency,

a delay adjustment circuit for adjusting phases between output signals from the plurality of sampling frequency conversion circuits and outputting the signals, an addition circuit for selecting and weighting two signals from a plurality of output signals from the delay adjustment circuit in accordance with the control signal, and a switching circuit for selecting one signal from a plurality of output signals from the delay adjustment circuit and an output signal from the addition circuit in accordance with the control signal.

In this case, the switching circuit may switch a signal before switching of output signals from the delay adjustment circuit to an output signal from the addition circuit at a timing set in consideration of a delay time in the delay adjustment circuit from a switching timing designated by the control signal, output the output signal from the addition circuit for a predetermined interval, and then output the signal after switching.

In addition, the above speech switching apparatus may further comprise a speech decoding circuit for decoding a plurality of signals sampled from one bit stream with different sampling frequencies, and outputting the signals as the plurality of input signals to the sampling frequency conversion circuit or the delay adjustment circuit; and one signal is selected from a plurality of output decoded signals from the

speech decoding circuit in accordance with a bit rate at the time of reception and the control signal and output.

The above speech switching apparatus may further comprise a bit stream switching circuit for receiving bit streams obtained by multiplexing a plurality of bit streams in which a plurality of types of signals having different sampling frequencies, and switching/outputting the bit streams to a plurality of output terminals in accordance with types of bit streams, and a plurality of speech decoding circuits for decoding the respective bit streams output from the bit stream switching circuit, and outputting the bit streams as the plurality of input signals to the sampling frequency conversion circuit or the delay adjustment circuit, and one signal may be selected from output decoded signals from the plurality of speech decoding circuits in accordance with the control signal and output.

Brief Description of Drawings

Fig. 1 is a view showing the arrangement of the first embodiment of the present invention;

Fig. 2 is a view showing the arrangement of the second embodiment of the present invention;

Fig. 3 is a view showing the arrangement of the third embodiment of the present invention;

Fig. 4 is a view showing the arrangement of the fourth embodiment of the present invention;

Fig. 5 is a view showing the arrangement of

the fifth embodiment of the present invention;

Fig. 6 is a view showing the arrangement of the sixth embodiment of the present invention; and

Fig. 7 is a view showing an example of the arrangement of a conventional speech switching apparatus.

Best Mode of Carrying Out the Invention

The mode of carrying out the present invention will be described below. According to the present invention, when digital speech signals having different sampling frequencies are to be reconstructed/switched, in order to eliminate interruptions in reconstructed speech, a plurality of digital speech signals having different sampling frequencies are converted into signals having the same sampling frequency, and the resultant phases are adjusted, thereby reconstructing the signals.

More specifically, the present invention includes a sampling frequency conversion circuit (1 in Fig. 1) for converting the sampling frequencies of digital speech signals and a delay adjustment circuit (2 in Fig. 1) for adjusting a phase shift caused by sampling frequency conversion between a plurality of digital speech signals.

To eliminate discontinuity caused between samples when digital speech signals having the same sampling frequency and different signal bandwidths are continuously reconstructed, the digital speech signals

before and after switching are weighted/added for a predetermined interval first, and then are switched/reconstructed. More specifically, the present invention includes a sampling frequency conversion circuit (1 in Fig. 3), a delay adjustment circuit (2 in Fig. 3), an addition circuit (6 in Fig. 3) for weighting/adding output signals from the delay adjustment circuit for a predetermined interval, and a switching circuit (7 in Fig. 3) for switching output signals from the addition circuit in accordance with a control signal after outputting an output signal from the addition circuit for the interval.

According to the present invention, the sampling frequency conversion circuit and delay adjustment circuit make digital signals before and after switching have the same sampling frequency and phase. This reduces the tendency to cause interruptions in reconstructed speech without requiring sampling frequency setting in a D/A circuit.

In addition, according to the present invention, the addition circuit weights/adds digital signals before and after switching to reduce discontinuity between the final sample of a speech signal before switching and the first sample in the interval as compared with a case where no weighting/adding operation is performed. The switching circuit performs switching after an output signal from

the addition circuit is output for a predetermined interval. This reduces discontinuity between samples at the start and end of the interval, and hence reduces the tendency to produce strange sounds in reconstructed speech.

To describe the above mode in more detail, the embodiments of the present invention will be described with reference to the accompanying drawings.

Fig. 1 is a block diagram showing the arrangement of the first embodiment of the present invention. Referring to Fig. 1, in the first embodiment of the present invention, two types of speech signals (first and second speech signals) having different sampling frequencies (e.g., 8 kHz and 16 kHz) and a control signal for instructing to reconstruct one of the two types of speech signals are input, and the speech signals are switched and reconstructed in accordance with the control signal.

A sampling frequency conversion circuit 1 performs sampling frequency conversion to match the sampling frequency of the first speech signal to the sampling frequency of the second speech signal (e.g., converts the sampling frequency from 8 kHz to 16 kHz), and outputs the resultant signal to a delay adjustment circuit 2. In this case, the sampling frequency conversion circuit 1 performs frequency conversion by using a frequency-multiplying or frequency-dividing

circuit or performing interpolation or decimation processing. This frequency conversion is performed by using a known circuit. For its operation, refer to, for example, P.P. Vaidyanathan, "Multirate Systems and Filter Banks", Section 4. 1. 1 (Figure 4.1-8).

Owing to the processing performed by the sampling frequency conversion circuit 1, the output signal undergoes a phase delay with respect to the input signal. Let D be the delay time in this case.

The delay adjustment circuit 2 outputs the signal obtained by delaying the input second speech signal by the delay time D using a delay circuit (not shown) and the output signal from the sampling frequency conversion circuit 1 to a switching circuit 3. As the delay circuit, an arbitrary circuit such as an inverter array or delay line is used.

The switching circuit 3 receives the first speech signal having undergone sampling frequency conversion and the second delay signal having undergone delay adjustment from the delay adjustment circuit 2, switches the two types of speech signals, in consideration of the delay time D, in accordance with the control signal, and outputs the resultant signal to a D/A conversion circuit 4.

The D/A conversion circuit 4 converts the input digital speech signal into an analog signal and outputs it. The analog signal is provided for a user

through a speaker, headphone, or the like.

Fig. 2 is a block diagram showing the arrangement of the second embodiment of the present invention. The second embodiment of the present invention additionally has a sampling frequency circuit 5 for performing sampling frequency conversion of a second speech signal, as compared with the first embodiment. A sampling frequency conversion circuit 1 converts the sampling frequency of a first speech signal into a predetermined sampling frequency, and outputs the resultant signal to a delay adjustment circuit 2. Likewise, the sampling frequency conversion circuit 5 converts the sampling frequency of the second speech signal into a predetermined sampling frequency, and outputs the resultant signal to the delay adjustment circuit 2. Let D1 be the delay time produced in the sampling frequency conversion circuit 1, and D2 be the delay time produced in the sampling frequency conversion circuit 5.

The delay adjustment circuit 2 performs delay adjustment to set the first and second speech signals having undergone sampling frequency conversion in phase, and outputs the resultant signals to a switching circuit 3.

For delay adjustment, letting D be one of the delay times D1 and D2 which is longer than the other, the two signals are delayed by the same time, i.e., the

delay time D, using a delay circuit (not shown).

The switching circuit 3 receives the first and second speech signals having undergone sampling frequency conversion and delay adjustment from the delay adjustment circuit 2, switches the two types of speech signals, in consideration of the delay time D, in accordance with the control signal, and outputs the resultant signal to a D/A conversion circuit 4.

The D/A conversion circuit 4 converts the input digital speech signal into an analog signal and outputs it. The analog signal is provided for a user through a speaker, headphone, or the like.

In this embodiment, for example, when the sampling frequencies of the first and second speech signals are 8 kHz and 12 kHz, respectively, the sampling frequencies of the first and second speech signals are converted into 24 kHz. This makes it possible to further reduce the processing amount of sampling frequency conversion as compared with the first embodiment in which only the sampling frequency of the first speech signal is converted into 12 kHz.

Fig. 3 is a block diagram showing the arrangement of the third embodiment of the present invention. Referring to Fig. 3, the third embodiment of the present invention further includes an addition circuit 6 as compared with the first embodiment. In addition, the operation of a switching circuit 7 differs

from that in the first embodiment.

A sampling frequency conversion circuit 1 performs sampling frequency conversion to match the sampling frequency of a first speech signal to the sampling frequency of a second speech signal, and outputs the resultant signal to a delay adjustment circuit 2. Let the delay time produced in the sampling frequency conversion circuit 1 be D. The delay adjustment circuit 2 outputs to the addition circuit 6 the signal obtained by delaying the input second speech signal by the delay time D and the output signal from the sampling frequency conversion circuit 1.

The addition circuit 6 weights/adds the first speech signal having undergone sampling frequency conversion and the second speech signal having undergone delay adjustment, and outputs the resultant signal to the switching circuit 7.

For example, in weighting/adding operation, if signals before and after switching are given by

$$S1(n),\ S2(n),\ n = 0, 1, \ldots, T-1$$

then, an output signal S3(n) from the addition circuit 5 is given by

$$S3(n) = (n/(T-1))S2(n) + ((T-1 - n)/(T-1))S1(n),$$
$$n = 0, 1, \ldots, T-1, \qquad \ldots(1)$$

where T is a sample count which represents intervals at which output signals from the addition circuit are used and is determined for each sampling frequency of an

input speech signal.

In addition, as signals before and after switching, either the first speech signal having undergone sampling frequency conversion or the second speech signal having undergone delay adjustment is assigned.

The switching circuit 7 receives the first speech signal having undergone sampling frequency conversion, the second speech signal having undergone delay adjustment, the output signal from the addition circuit 6, and a control signal, and switches the signal to be output from a signal S1(n) before switching to the output signal S3(n) from the addition circuit 6 at a timing set, in consideration of the delay time D, on the basis of the switching timing designated by the control signal. The switching circuit 7 then outputs the signal S1(n) after switching to a D/A conversion circuit after outputting the signal S3(n) for a predetermined interval.

A D/A conversion circuit 4 converts the input digital speech signal into an analog signal and outputs it. The analog signal is provided for a user through a speaker, headphone, or the like.

Fig. 4 is a block diagram showing the arrangement of the fourth embodiment of the present invention. Referring to Fig. 4, the fourth embodiment of the present invention further includes an addition circuit 6 as compared with the second embodiment. In

addition, the operation of a switching circuit 7 differs from that in the second embodiment.

In the fourth embodiment of the present invention, the operations of the addition circuit 6 and switching circuit 7 are the same as those described in the third embodiment.

A sampling frequency conversion circuit 1 converts the sampling frequency of a first speech signal into a predetermined sampling frequency (e.g., 24 kHz), and outputs the resultant signal to a delay adjustment circuit 2. Likewise, a sampling frequency conversion circuit 5 converts the sampling frequency of a second speech signal into a predetermined sampling frequency, and outputs the resultant signal to the delay adjustment circuit 2. Let D1 be the delay time produced in the sampling frequency conversion circuit 1, and D2 be the delay time produced in the sampling frequency conversion circuit 5. The delay adjustment circuit 2 performs delay adjustment to set the first and second speech signals having undergone sampling frequency conversion in phase, and outputs the resultant signals to the addition circuit 6 and switching circuit 7. For example, in delay adjustment, letting D be one of the delay times D1 and D2 which is longer than the other, the two signals are delayed by the delay time D.

The addition circuit 6 weights/adds the first and second speech signals having undergone sampling

frequency conversion and delay adjustment, and outputs the resultant signal to the switching circuit 7.

For example, in weighting/adding operation, equation (1) is used. In this case, as signals S1(n) and S2(n) before and after switching, one of the first and second speech signals having undergone sampling frequency conversion and delay adjustment is assigned.

The switching circuit 7 receives the first and second speech signals having undergone sampling frequency conversion and delay adjustment, the output signal from the addition circuit 6, and a control signal, and switches the signal to be output from the signal S1(n) before switching to an output signal S3(n) from the addition circuit 5 at a timing set, in consideration of the delay time D, on the basis of the switching timing designated by the control signal. The switching circuit 7 then outputs the signal S1(n) after switching to a D/A conversion circuit after the signal S3(n) is output for a predetermined interval.

A D/A conversion circuit 4 converts the input digital speech signal into an analog signal and outputs it. The analog signal is provided for a user through a speaker, headphone, or the like.

Fig. 5 is a block diagram showing the arrangement of a speech switching apparatus according to the fifth embodiment of the present invention, which is a combination of a speech decoding circuit 8 and the

arrangement of the third embodiment. Referring to Fig. 5, in the fifth embodiment of the present invention, the bandwidth-hierarchized speech decoding circuit 8 outputs as first and second digital speech signals digital speech signals obtained by decoding an input bit stream to a sampling frequency conversion circuit 1 and delay circuit 2.

The bandwidth-hierarchized speech decoding circuit 8 outputs, to an addition circuit 6 and switching circuit 7, a control signal for instructing which one of two types of speech signals is to be reconstructed.

In this case, the bit stream is constituted by a fundamental portion indispensable to decoding of compressed speech signal information and an expansion portion for improving the quality of the speech signal by expanding the bandwidth.

When, therefore, the bandwidth-hierarchized speech decoding circuit 8 receives only a fundamental portion, it decodes the portion into a speech signal with a narrow bandwidth (e.g., a digital signal having a sampling frequency of 8 kHz), and outputs it to the sampling frequency conversion circuit 1.

When this circuit also receives an expansion portion, it decodes the signal into a speech signal with a winder bandwidth (e.g., a digital signal having a sampling frequency of 16 kHz), and outputs it to the

delay adjustment circuit 2.

For the decoding operation of the bandwidth-hierarchized speech decoding circuit 8, refer to, for example, Japanese Patent Laid-Open No. 11-30997.

When the bandwidth-hierarchized speech decoding circuit 8 receives the expansion portion of a bit stream as well as the fundamental portion, the circuit can simultaneously obtain a plurality of decoded signals, i.e., a decoded signal obtained by using only the fundamental portion and a signal obtained by using both the fundamental portion and the expansion portion.

Assume that in this embodiment, a decoded signal using only the fundamental portion of a bit stream is always obtained and output to the delay adjustment circuit 2.

The operations of the sampling frequency conversion circuit 1, delay adjustment circuit 2, addition circuit 6, switching circuit 7, and D/A conversion circuit 4 are the same as those in the second embodiment, and hence a description thereof will be omitted.

Fig. 6 is a block diagram showing the arrangement of a speech switching apparatus according to the sixth embodiment of the present invention, which is a combination of a plurality of speech decoding circuits and the first embodiment described above. Referring to Fig. 6, in the sixth embodiment of the present invention,

a bit stream switching circuit 11 receives a bit steam obtained by multiplexing a plurality of bit streams as compressed signals having different sampling frequencies, and outputs the input bit stream to a first speech decoding circuit 9 or second speech decoding circuit 10 depending on the type of the received bit stream.

In this case, as a method of multiplexing bit streams, a method of simultaneously multiplexing a plurality of bit streams or a method of switching and multiplexing them may be used. In the former method, two types of speech signals are simultaneously decoded from two types of bit streams. In the latter method, a speech signal is decoded from only one of the bit streams. Assume that in this embodiment, a bit stream obtained by switching/multiplexing a plurality of bit streams is input.

The bit stream switching circuit 11 outputs, to a switching circuit 3, a control signal for instructing which one of the two types of speech signals is to be reconstructed.

The first speech decoding circuit 9 outputs a speech signal (e.g., a digital signal having a sampling frequency of 8 kHz) obtained by decoding a bit stream having a lower bit rate (e.g., 8 kbit/s) than in the second speech decoding circuit 10 as a first digital speech signal to a sampling frequency conversion circuit 1.

The second speech decoding circuit 10 outputs a speech signal (e.g., a digital signal having a sampling frequency of 16 kHz) obtained by decoding a bit stream having a higher bit rate (e.g., 16 kbit/s) than in the first speech decoding circuit 9 as a second digital speech signal to a delay adjustment circuit 2.

In this case, for the first speech decoding circuit 9 and second speech decoding circuit 10, refer to, for example, Japanese Patent Laid-Open No. 10-207496.

The operations of the sampling frequency conversion circuit 1, delay adjustment circuit 2, switching circuit 3, and D/A conversion circuit 4 are the same as those in the first embodiment, and a description thereof will be omitted.

Fig. 5 shows a combination of the bandwidth-hierarchized speech decoding circuit and the arrangement of the third embodiment. Fig. 6 shows a combination of the plurality of speech decoding circuits and the arrangement of the first embodiment. Obviously, however, the above embodiments may be arbitrarily combined with each other.

In the third and fourth embodiments, since the addition circuit simultaneously requires a plurality of signals, when the first and second speech signals are switched, the two signals must overlap each other.

In the third and fourth embodiments each combined with the speech decoding circuit, therefore,

the apparatus must be combined with a bandwidth-hierarchized speech decoding circuit. Alternatively, if a plurality of speech decoding circuits are used, an input bit stream must be the one obtained by simultaneously multiplexing a plurality of bit streams.

Each embodiment exemplifies the case where two type of input speech signals are processed. An apparatus designed to process three or more types of input speech signals can be realized by adding necessary numbers of sampling frequency conversion circuits and input/output lines to be connected thereto.

As has been described above, according to the present invention, strange sounds that are produced when a plurality of different speech signals are reconstructed and switched can be reduced.

This is because, in the present invention, matching the sampling frequencies and phases of signals before and after switching of a plurality of speech signals obviates the necessity to change the sampling frequency settings.

In addition, by weighting/adding speech signals before and after switching for a predetermined interval, discontinuity between samples at the start and end of the interval can be reduced.

C L A I M S

1. A speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising:

at least one sampling frequency conversion circuit for converting a sampling frequency of at least one of the plurality of input signals;

a delay adjustment circuit for adjusting a phase of the input signal, of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit and a phase of the remaining input signal, and outputting the signals; and

a switching circuit for selecting one of a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

2. A speech switching apparatus according to claim 1, characterized in that said delay adjustment circuit makes an adjustment to match the phase of the signal whose sampling frequency is converted to the phase of the remaining input signal.

3. A speech switching apparatus according

to claim 1, characterized in that said switching circuit switches outputs at a timing set in consideration of a delay time in said delay adjustment circuit with respect to a switching timing designated by the control signal.

4. A speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising:

a plurality of sampling frequency conversion circuits for converting sampling frequencies of the plurality of input signals to a predetermined frequency;

a delay adjustment circuit for adjusting phases between output signals from said plurality of sampling frequency conversion circuits and outputting the signals; and

a switching circuit for selecting one signal from a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

5. A speech switching apparatus according to claim 4, characterized in that said delay adjustment circuit makes an adjustment to match the phase of the signal whose sampling frequency is converted to the phase of the remaining input signal.

6. A speech switching apparatus according to claim 4, characterized in that said switching circuit switches outputs at a timing set in consideration of a delay time in said delay adjustment circuit with respect to a switching timing designated by the control signal.

7. A speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising:

at least one sampling frequency conversion circuit for converting a sampling frequency of at least one of the plurality of input signals;

a delay adjustment circuit for adjusting a phase of the input signal, of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit and a phase of the remaining input signal, and outputting the signals;

an addition circuit for selecting and weighting two signals from a plurality of output signals from said delay adjustment circuit in accordance with the control signal; and

a switching circuit for selecting one signal from a plurality of output signals from said delay

adjustment circuit and an output signal from said addition circuit in accordance with the control signal.

8. A speech switching apparatus according to claim 7, characterized in that said switching circuit switches a signal before switching of output signals from said delay adjustment circuit to an output signal from said addition circuit at a timing set in consideration of a delay time in said delay adjustment circuit from a switching timing designated by the control signal, outputs the output signal from said addition circuit for a predetermined interval, and then outputs the signal after switching.

9. A speech switching apparatus for receiving a plurality of input signal sampled with a plurality of different sampling frequencies and a control signal for designating a signal of the plurality of input signals which is to be reconstructed, and selecting and outputting one of the plurality of input signals in accordance with the control signal, characterized by comprising:

a plurality of sampling frequency conversion circuits for converting sampling frequencies of the plurality of input signals to a predetermined frequency;

a delay adjustment circuit for adjusting phases between output signals from said plurality of sampling frequency conversion circuits and outputting the signals;

an addition circuit for selecting and weighting two signals from a plurality of output signals from said delay adjustment circuit in accordance with the control signal; and

a switching circuit for selecting one signal from a plurality of output signals from said delay adjustment circuit and an output signal from said addition circuit in accordance with the control signal.

10. A speech switching apparatus according to claim 9, characterized in that said switching circuit switches a signal before switching of output signals from said delay adjustment circuit to an output signal from said addition circuit at a timing set in consideration of a delay time in said delay adjustment circuit from a switching timing designated by the control signal, outputs the output signal from said addition circuit for a predetermined interval, and then outputs the signal after switching.

11. A switching apparatus according to claim 1, characterized in that

said apparatus further comprises a speech decoding circuit for decoding a plurality of signals sampled from one bit stream with different sampling frequencies, and outputting the signals as the plurality of input signals to said sampling frequency conversion circuit or said delay adjustment circuit; and

one signal is selected from a plurality of

output decoded signals from said speech decoding circuit in accordance with a bit rate at the time of reception and the control signal and output.

12. A switching apparatus according to claim 4, characterized in that

said apparatus further comprises a speech decoding circuit for decoding a plurality of signals sampled from one bit stream with different sampling frequencies, and outputting the signals as the plurality of input signals to said plurality of sampling frequency conversion circuits; and

one signal is selected from a plurality of output decoded signals from said speech decoding circuit in accordance with a bit rate at the time of reception and the control signal and output.

13. A speech switching apparatus according to claim 1, characterized in that

said apparatus further comprises a bit stream switching circuit for receiving bit streams obtained by multiplexing a plurality of bit streams in which a plurality of types of signals having different sampling frequencies, and switching/outputting the bit streams to a plurality of output terminals in accordance with types of bit streams, and

a plurality of speech decoding circuits for decoding the respective bit streams output from said bit stream switching circuit, and outputting the bit streams

as the plurality of input signals to said sampling frequency conversion circuit or said delay adjustment circuit, and

one signal is selected from output decoded signals from said plurality of speech decoding circuits in accordance with the control signal and output.

14. A speech switching apparatus according to claim 1, characterized in that

said apparatus further comprises a bit stream switching circuit for receiving bit streams obtained by multiplexing a plurality of bit streams in which a plurality of types of signals having different sampling frequencies, and switching/outputting the bit streams to a plurality of output terminals in accordance with types of bit streams, and

a plurality of speech decoding circuits for decoding the respective bit streams output from said bit stream switching circuit, and outputting the bit streams as the plurality of input signals to said plurality of sampling frequency conversion circuits, and

one signal is selected from output decoded signals from said plurality of speech decoding circuits in accordance with the control signal and output.

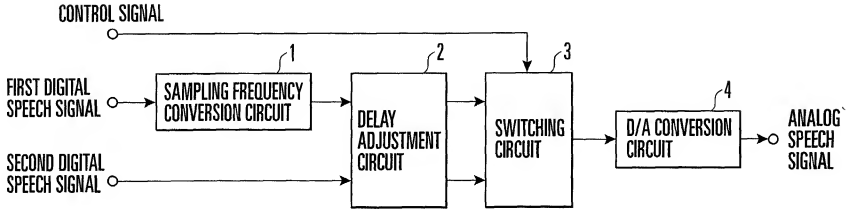

FIG. 1

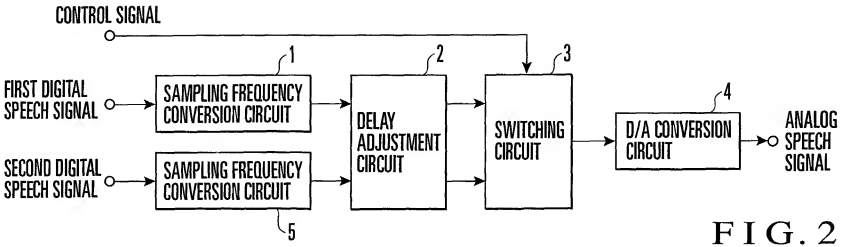

FIG. 2

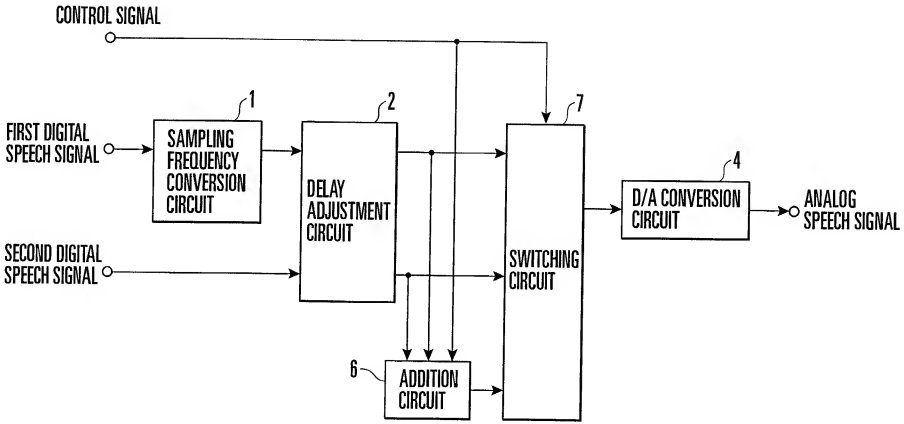

FIG. 3

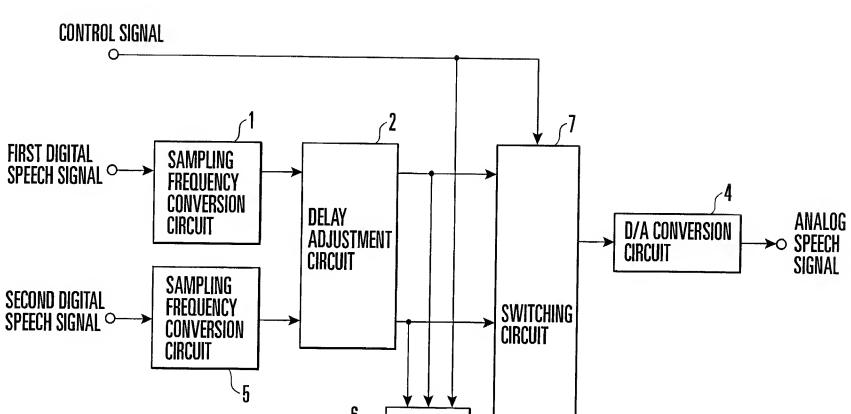

FIG. 4

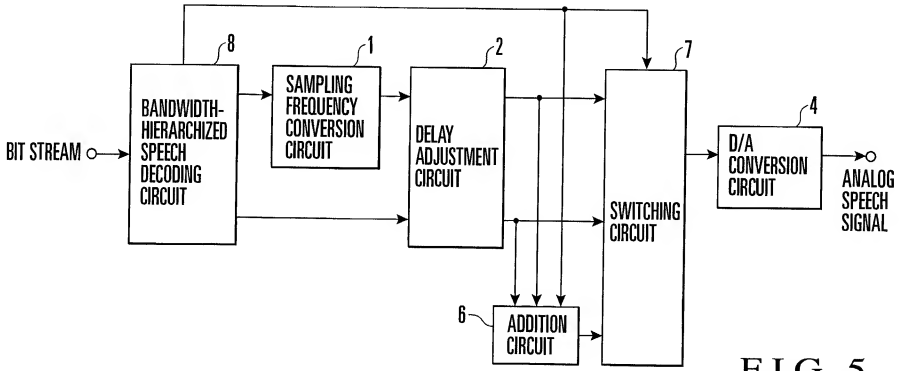

FIG. 5

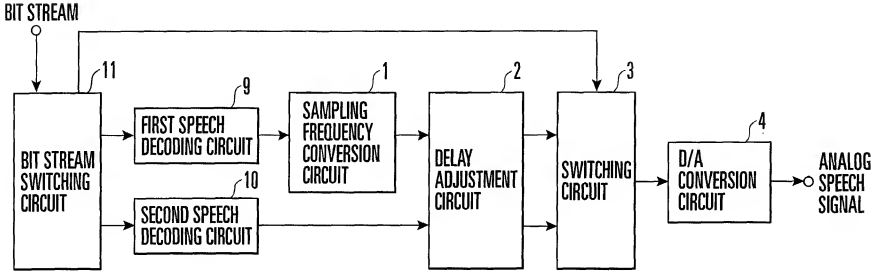

FIG. 6

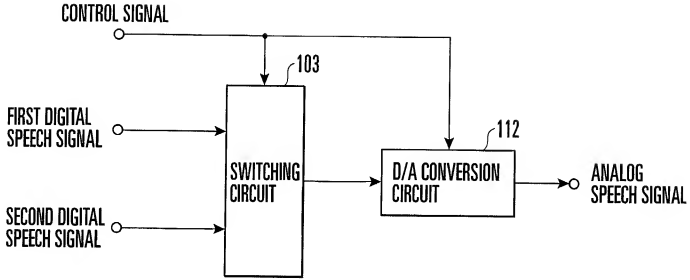

FIG. 7

UNITED STATES OF AMERICA
COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

OPGS FILE NO. P1647-141

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Speech Switching Apparatus

the specification of which is attached hereto, unless the following box is checked:

☒ was filed on May 19, 2000 as United States patent Application Number or PCT International patent application number PCT/JP00/03230 and was amended on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Japan	164665/1999	11,06,1999	YES ☒ NO ☐
			YES ☐ NO ☐
			YES ☐ NO ☐

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	STATUS *(patented, pending, abandoned)*

I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063, James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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RESIDENCE *(City and either State or Foreign Country)*		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		
FULL NAME OF THIRD JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE
RESIDENCE *(City and either State or Foreign Country)*		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		

☐ CONTINUED ON PAGE 2